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Voltage Controlled Oscillator (VCO) Design of High-Performance CMOS Voltage-Controlled Oscillators High-Frequency Integrated Circuits A Digital Voltage-controlled Oscillator for Phase Lock Loops Voltage Controlled Oscillator (VCO) Technology Design of VCO-based ADCs VCO-Based Quantizers Using Frequency-to-Digital and Time-to-Digital Converters A High Speed Integrated Voltage Controlled Oscillator in Commercial CMOS Technology The Voltage-controlled Oscillator Design of Monolithic Emitter Degenerated Voltage-controlled Oscillators Switchable Dual Mode Voltage Controlled Oscillator Distributed Voltage Controlled Oscillator A Voltage Controlled Oscillator Implemented with Double Injection Diodes VLSI Design and Test High Frequency CMOS Voltage-controlled Oscillator Design of a Voltage Controlled Oscillator Low Phase Noise, Voltage Controlled Oscillator in Microstrip A Design and Analysis of High Performance Voltage Controlled Oscillators Low-power Low-phase-noise Voltage-controlled Oscillator Design Time-encoding VCO-

ADCs for Integrated Systems-on-Chip A Voltage Controlled Oscillator Circuit Using Single Channel MOS Technology Voltage-controlled Oscillator (VCO) Design Used in Phase-locked Loops (PLLs) Based on CMOS Process A Voltage Controlled Oscillator/Mixer A Wide Range Voltage Controlled Oscillator Dual Switched Voltage Controlled Oscillator and It's [sic] Characterization A Low Power Low Phase Noise Voltage Controlled Oscillator Analog CMOS Voltage Controlled Oscillator (VCO) in Phase Locked Loop (PLL) Comparative Analysis of Various Cmos Based VCO Analysis of Nonlinearities in a Voltage-controlled Oscillator Design of a 2,4 GHz CMOS Voltage Controlled Oscillator Ku Band Rotary Traveling-wave Voltage Controlled Oscillator Microelectronics, Electromagnetics and Telecommunications Linearity of the L-C Voltage Controlled Oscillator Design, Construction and Testing of a Voltage Controlled Oscillator Design of a Fully Integrated Voltage-controlled Oscillator Low Phase Noise Voltage-controlled Oscillator Design A Digital Voltage-controlled Oscillator for Phase Lock Loops Automatic Generation of an LC Voltage Controlled Oscillator Voltage Controlled Oscillator Based on High-k Materials for Phase Locked Loop Applictions Precise Frequency

Control of the Voltage Controlled Oscillator Using Finite Digital Word Lengths

Two kinds of voltage-controlled oscillators (VCO)--active inductor based VCO and LC cross-coupled VCO--are studied in this work. Although the phase noise performance is not competitive, the proposed active inductor based VCO provide an alternative method to VCO design with very small chip area and large tuning range. The measurement shows a test oscillator based on active inductor topology successfully oscillates near 530MHz band. The phase noise of the widely used LC cross-coupled VCO is extensively investigated in this work. Under the widely used power dissipation and chip area constraints, a novel optimization procedure in LC oscillator design centered on a new inductance selection criterion is proposed. This optimization procedure is based on a physical phase noise model. From it, several closed-form expressions are derived to describe the phase noise generated in the LC oscillators, which indicate that the phase noise is proportional to the L2· gL3 factor. The minimum value of this factor for an area-limited spiral inductor is proven to monotonically decrease with increasing inductance, suggesting a larger inductance is helpful to reduce the phase noise in LC VCO design. The validity of the optimization procedure is proven by simulations. Two test chips are designed and measured. Voltage-controlled oscillator (VCO) plays a key role in determination of the link budget of wireless communication, and consequently the performance of the transceiver. Lowering the noise contribution from the VCO to the entire system is always challenging and remains the active research area. Motivated by high demands for the low-phase noise, low-power consumption VCO in the application of 5G, radar-sensing system, implantable device, to name a few, this research focused on the design of a rotary travelling-wave oscillator (RTWO). A power conscious RTWO with reliable direction control of the wave propagation was investigated. The phase noise was analyzed based on the proposed RTWO. The phase noise reduction technique was introduced by using tail current source filtering technique in which a figure-8 inductors were employed. Three RTWO were implemented based on GF 130 nm standard CMOS process and TSMC 130 nm standard CMOS process. The first design was achieving 16-GHz frequency with power consumption of 5.8-mW with 190.3 dBc/Hz FoM at

1 MHz offset. The second and third design were operating at 14-GHz with a power consumption range of 13-18.4mW and 14.6-20.5mW, respectively. The one with filtering technique achieved FoM of 184.8 dBc/Hz at 1 MHz whereas the one without inudctor filtering obtained FoM of 180.8 dBc/Hz at 1 MHz offset based on simulation. The voltage-controlled oscillator (VCO) is one of the most important building blocks in data communication systems. The design of high performance monolithic integrated VCO is extremely challenging and is still an active research area. In this dissertation, the emitter degeneration technique is presented. The concept is first explained intuitively, refined later by more accurate models. The benefits of emitter degeneration are analytically proven, and also verified through simulation and experimentation. Design equations, design and layout guidelines are provided. Using SiGe BiCMOS technology, four VCOs and a clock recovery circuits are fabricated as strong evidence of the usefulness of this technique. Comparisons to recent publications are also conducted. The developed capacitive emitter degeneration technique is applicable to future VCOs because it is process independent, and its ability to simultaneously increase

oscillation frequency, tuning range while improving phase noise makes it an extremely powerful technique for high performance bipolar-transistor based VCO design. Abstract: The design of voltage-controlled Oscillators nowadays is all about being capable of operating at higher clock frequencies for the purpose of higher data rate, consuming less power for the purpose of longer battery life, and having better phase noise performance for the purpose of higher quality of wireless service and more efficient use of the available frequency spectrum since most of the wireless and mobile terminals that these VCOs work in are required to be able to operate in multiple RF standards to serve new generations of standards while being backward compatible with existing ones, leading to a demand for multi-standard multi-band radio operation that deals with high frequency RF signals that undergo different modulation schemes of different standards in different channels over a wide range of frequency band. A top-down system design from the PLL to the VCO is carried out to determine the specifications for a fully integrated dual-band voltage-controlled oscillator (VCO) designed for a Zero-IF WiMAX/WLAN receiver in a O.18tm CMOS technology with 1.8V supply voltage. A VCO employing a differential cross-coupled inductance-capacitance (LC) tank architecture is proposed to cover twice the desired frequency bands for WiMAX and WLAN standards in order to avoid load pulling between VCO frequency and incoming RF frequency. The switching between two bands is implemented by using two binary-weighted capacitor arrays while switching inside each sub-band is implemented by different digital control signal combinations for the binary-weighted capacitances. A phase noise of -120.7dB/Hz at 1MHz offset frequency is demonstrated for an oscillation frequency of 4.84GHz. The average power consumption of this VCO is 8.1mW. This VCO is developed as an IP (Intellectual Property) to be used in a fully integrated CMOS multi-standard WiMAX/WLAN radio allowing seamless roaming of handheld mobile devices between hotspots in future Wireless Metropolitan Area Network (WMAN). To compare the performance of ring oscillators to that of LC tank oscillators, the designs of two three-stage multiple-pass voltage-controlled ring oscillators with dual-delay paths are demonstrated where the differential delay cell utilizes both the primary loop delay and the negative skewed delay to increase the frequency of oscillation substantially and retain or even increase tuning range. Their phase noise performance is also improved by switching in and out the transistors periodically. In design I, the covered frequency range is from 0.74 GHz to 1.96 GHz, which translates to a tuning range of 90 % A phase noise of -104.995dBc/Hz is demonstrated for an oscillation frequency of 1.8535 GHz. Each stage draws a current of 4.963mA on average from a 1.8V power supply, resulting in a power consumption of 26.8mW. In design II, the covered frequency range is from 1.0478 GHz to 2.0022 GHz, which translates to a tuning range of 63%. The frequency-voltage curve is almost a perfect linear curve for V between OV and 0.9V. A phase noise of -110.O45dBc/Hz is demonstrated for an oscillation frequency of 2.00216 GHz. Each stage draws a current of 10.179mA on average from a 1.8V power supply, resulting in a power consumption of 55mW. A new technique for product mixing of an input signal with a locally generated reference by using a voltage controlled oscillator (VCO) is described and verified both mathematically and experimentally. The technique consists of frequency modulating the oscillator with the signal voltage. It is shown that for low-index frequency modulation by the signal, the sidebands of the oscillator produced by the signal are equivalent to those of a multiplicative mixer with a gain of approximately unity. The technique is particularly useful for synchronized IF correlator systems where a function generator can serve to generate the modulation waveform and act as a coherent detector simultaneously. (Modified author abstract). The explosive growth in wireless communication has driven research into low-cost, low-power and miniaturised wireless receivers. A low power and low phase noise voltage controlled oscillator (VCO) is one of the key components of transceiver systems. Close-in phase noise, responsible for jitter in time domain, is the most important parameter of a VCO as it results in inter-symbol interferences in high speed analogue to digital converters (ADCs). VCO phase noise also degrades system sensitivity and selectivity of wireless receivers. To improve battery life, VCO designs for wireless receivers must consume the least possible power. Hence, the primary aims of this research are to achieve a VCO with very low close-in phase noise and with low power consumption. Substantial research into VCO topologies and the design of on-chip passive elements has made on-chip complementary metal oxide semiconductor (CMOS) implementation of LC-tank VCO possible. However, the principle issues with CMOS LC-VCOs have been the unavailability of a high quality factor (Q) on-chip inductor and high flicker noise of active devices. This book demonstrates why highly-digital CMOS time-encoding analog-to-digital converters incorporating voltage-controlled oscillators (VCOs) and time-to-digital converters (TDCs) are a good alternative to traditional switched-capacitor S-D modulators for power-efficient sensor, biomedical and communications applications. The authors describe the theoretical foundations and design methodology of such time-based ADCs from the basics to the latest developments. While most analog designers might notice some resemblance to PLL design, the book clearly highlights the differences to standard PLL circuit design and illustrates the design methodology with practical circuit design examples. Describes in detail the design methodology for CMOS time-encoding analog-to-digital converters that can be integrated along with digital logic in a nanometer System on Chip; Assists analog designers with the necessary change in design paradigm, highlighting differences between designing time-based ADCs and traditional analog circuits like switched-capacitor converters and PLLs; Uses a highly-visual, tutorial approach to the topic, including many practical examples of techniques introduced. A transistor-level, design-intensive overview of high speed and high frequency monolithic integrated circuits for wireless and broadband systems from 2 GHz to 200 GHz, this comprehensive text covers high-speed, RF, mm-wave, and optical fibre circuits using nanoscale CMOS, SiGe BiCMOS, and III-V technologies. Step-by-step design methodologies, end-of chapter problems, and practical simulation and design projects are provided, making this an ideal resource for senior undergraduate and graduate courses in circuit design. With an emphasis on device-circuit topology interaction and optimization, it gives circuit designers and students alike an in-depth understanding of device structures and process limitations affecting circuit performance. This book constitutes the refereed proceedings of the 17th International Symposium on VLSI Design and Test, VDAT 2013, held in Jaipur, India, in July 2013. The 44 papers presented were carefully reviewed and selected from 162 submissions. The papers discuss the frontiers of design and test of VLSI components, circuits and systems. They are organized in topical sections on VLSI design, testing and verification, embedded systems, emerging technology. This book introduces the concept of voltage-controlled-oscillator (VCO)-based analog-to-digital converters (ADCs). Detailed explanation is given of this promising new class of high resolution and low power ADCs, which use time quantization as opposed to traditional analog-based (i.e. voltage) ADCs. Design of High-Performance CMOS Voltage-Controlled Oscillators presents a phase noise modeling framework for CMOS ring oscillators. The analysis considers both linear and nonlinear operation. It indicates that fast rail-to-rail switching has to be achieved to minimize phase noise. Additionally, in conventional design the flicker noise in the bias circuit can potentially dominate the phase noise at low offset frequencies. Therefore, for narrow bandwidth PLLs, noise up conversion for the bias circuits should be minimized. We define the effective Q factor (Qeff) for ring oscillators and predict its increase for CMOS processes with smaller feature sizes. Our phase noise analysis is validated via simulation and measurement results. The digital switching noise coupled through the power supply and substrate is usually the dominant source of clock jitter. Improving the supply and substrate noise immunity of a PLL is a challenging job in hostile environments such as a microprocessor chip where millions of digital gates are present. Today's complex electronic systems with billions of transistors on a single die are enabled by the aggressive scaling down of the device feature size at an exponential rate as predicted by the Moore's law. Digital circuits benefit from technology scaling to become faster, more energy efficient as well as more area efficient as the feature size is scaled down. Moreover, digital design also benefits from mature CAD tools that simplify the design and cross-technology porting of complex systems, leveraging on a cell-based design methodology. On the other hand, the design of analog circuits is getting increasingly difficult as the feature size scales down into the deep nanometer regime due to a variety of reasons like shrinking voltage headroom, reducing intrinsic gain of the devices, increasing noise coupling between circuit nodes due to shorter distances etc. Furthermore, analog circuits are still largely designed with a full custom design ow that makes their design and porting tedious, slow, and expensive. In this context, it is attractive to consider realizing analog/mixed-signal circuits using standard digital components. This leads to scaling-friendly mixed-signal blocks that can be designed and ported using the existing CAD framework available for digital design. The concept is already being applied to mixed-signal components like frequency synthesizers where all-digital architectures are synthesized using standard cells as basic components. This can be extended to other mixed-signal blocks like digital-to-analog and analog to- digital converters as well, where the latter is of particular interest in this thesis. A voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) is an attractive architecture to achieve all-digital analog-to digital conversion due to favorable properties like shaping of the quantization error, inherent anti-alias filtering etc. Here a VCO operates as a signal integrator as well as a quantizer. A converter employing a ring oscillator as the VCO lends itself to an all-digital implementation. In this dissertation, we explore the design of VCO-based ADCs synthesized using digital standard cells with the long-term goal of achieving high performance data converters built from low accuracy switch components. In a first step, an ADC is designed using vendor supplied standard cells and fabricated in a 65 nm CMOS process. The converter delivers an 8-bit ENOB over a 25 MHz bandwidth while consuming 3.3 mW of power resulting in an energy efficiency of 235 fJ/step (Walden FoM). Then we utilize standard digital CAD tools to synthesize converter designs that are fully described using a hardware description language. A polynomial-based digital post-processing scheme is proposed to correct for the VCO nonlinearity. In addition, pulse modulation schemes like delta modulation and asynchronous sigma-delta modulation are used as a signal pre-coding scheme, in an attempt to reduce the impact of VCO nonlinearity on converter performance. In order to investigate the scaling benefits of all-digital data conversion, a VCO-based converter is designed in a 28 nm CMOS process. The design delivers a 13.4-bit ENOB over a 5 MHz bandwidth achieving an energy efficiency of 4.3 fJ/step according to post-synthesis schematic simulation, indicating that such converters have the potential of achieving good performance in deeply scaled processes by exploiting scaling benefits. Furthermore, large conversion errors caused by non-ideal sampling of the oscillator phase are studied. An encoding scheme employing ones counters is proposed to code the sampled ring oscillator output into a number, which is resilient to a class of sampling induced errors modeled by temporal reordering of the transitions in the ring. The proposed encoding reduces the largest error caused by random reordering of up to six subsequent bits in the sampled signal from 31 to 2 LSBs. Finally, the impact of process, voltage, and temperature (PVT) variations on the performance while operating the converter from a subthreshold supply is investigated. PVT-adaptive solutions are suggested as a means to achieve energy-efficient operation over a wide range of PVT conditions. A Voltage Controlled Oscillator (VCO) is used to generate a signal with a frequency that is a function of an input voltage amplitude, and is an integral part of circuits such as phase locked loops, frequency synthesizers, down conversion receivers, and clock generators. A typical design flow for a VCO involves architecture selection based on specification, calculation of circuit parameters, simulation, and iterations of circuit parameters based on the simulation result. In such a design flow, changes in specification or process can lead to significant redesign. This report focuses on a C++ based LC VCO generation software that seeks to automate the design process and that includes calculation of circuit parameters, creation of Spectre netlist, invocation of simulation, automated checking of the result, and a feedback mechanism to modify circuit parameters until the design can converge to the desired specification. Object Oriented Programming principles such as inheritance, polymorphism, encapsulation, class abstraction are exercised to maximize reusability and portability to other projects which may require different foundry device models and supply voltages. The book discusses the latest developments and outlines future trends in the fields of microelectronics, electromagnetics and telecommunication. It contains original research works presented at the International Conference on Microelectronics, Electromagnetics and Telecommunication (ICMEET 2018), organised by GVP College of Engineering (A), Andhra Pradesh, India. The respective papers were written by scientists, research scholars and practitioners from leading universities, engineering colleges and R&D institutes from all over the world, and share the latest breakthroughs in and promising solutions to the most important issues facing today’s society.

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